REMARKS

Claims 1-9 remain pending in this application with claims 1-5 and 7-9 being amended by this Response.

Objection to the Specification

The specification stands objected to as not including the proper headings. The specification has been amended in accordance with the comments of the Examiner to add the proper headings. In view of the amendments to the specification it is respectfully submitted that this objection is satisfied and should be withdrawn.

Objection to Claims 1 and 3-9

Claims 1 and 3-9 stand objected to for certain informalities. In response to the comments of the Examiner, claims 1, 3-5 and 7-9 have been formally amended to correct typographical errors. In view of the amendments to the claims it is respectfully submitted that this objection is satisfied and should be withdrawn.

Rejection of claims 1-6 under 35 U.S.C. 102(b)

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Shinya (U.S. Patent No. 5,170,158).

The present claimed invention recites an arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device. The arrangement includes a plurality of semiconductor switches, each having a first terminal, a second terminal and a third terminal. A first bus is coupled to a first plurality of terminals for communicating corresponding signals. A plurality of local buses are separated from one another for communicating corresponding signals. A given local bus has a first bus section coupled to a second plurality of terminals associated with the given local bus and extends in a manner to cross over the first bus. A second bus section extends from the first bus section and has conductors thereof coupled in a local, clustering bus arrangement to the

second terminals of switches associated with the given local bus of the plurality of switches. The associated switches have the third terminals thereof coupled to consecutively disposed column conductors, respectively, of the array.

The inventive concept of the present invention relates to the structure of the data and control lines to minimize the number of crossovers. Minimizing the number of crossovers of the input bussing structure associated with the N selection parallel conductors and the input biasing structure associated with the M brightness information carrying parallel conductors as in the present claimed invention substantially eliminates the significant capacitive loads formed between the crossing conductors thereby minimizing capacitance shorting failures, unwanted crosstalk among the brightness information carrying conductors and excessive dynamic power dissipation.

Shinya discloses a display device. The device includes a driver circuit for driving data lines in a matrix display panel according to input digital signals. The driver circuit includes a number of digital-to-analog converters, the number of converters being less than the number of pixels. The converters are used to sequentially convert portions of the input digital image signal corresponding to one horizontal scanning line. Shinya neither discloses NOT TRUE nor suggests a first/control bus connected to the first terminal of each of the plurality of switches as in the present claimed invention. Furthermore, unlike the present claimed invention, the plurality of local buses shown and described in Shinya cross each of the plurality of first buses. This is unlike the present claimed invention wherein the first bus section of the plurality of local buses cross only the first/control bus. Thus, Shinya teaches away from the present claimed invention which is designed to minimize the number of crossovers of the local busses and the control buses. AS CLAIMED

In view of the above remarks and amendments to the claims clarifying the present claimed invention it is respectfully submitted that Shinya does not anticipate the present claimed invention. It is thus further respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of claims 7-9 under 35 USC 102(b)

Claims 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al. (U.S. Patent No. 5,113,181).

Claims 7-9 stand rejected as not being novel in view of Inoue et al. Claims 7-9 include similar limitations to claim 1, discussed above. Inoue et al. discloses a display apparatus including a plurality of pixels arranged in rows and columns. The apparatus includes a plurality of first control lines connecting a column of pixels in common and a plurality of second control lines connecting a row of pixels in common. The first control lines are divided into a plurality of blocks. The first control lines in each block is connected by a third control line. A switching element is disposed at each connection between third and first control lines. The plurality of first control lines cross over each of the plurality of second control lines as is clearly seen in Figures 2 and 6. This is unlike the present claimed invention wherein the first bus section of the plurality of local buses cross over only the first/control bus. Thus, similarly to Shinya, Inoue et al. also teaches away from the present claimed invention which is designed to minimize the number of crossovers of the local busses and the control buses.

In view of the above remarks and amendments to the claims clarifying the present claimed invention it is respectfully submitted that Inoue et al. does not anticipate the present claimed invention. It is thus further respectfully submitted that this rejection is satisfied and should be withdrawn.

Since the present claims set forth the present invention patentably and distinctly, and are not taught by the cited art either taken alone or in combination, this response is believed to place this case in condition for allowance and the Examiner is respectfully requested to reconsider the matter, and to allow all of the claims in this case.

Should the Examiner feel that anything further is necessary to place this application in condition for allowance he is respectfully requested to contact applicants attorney at the telephone number listed below.

No other fee is believed due. However, if an additional fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,
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Patent Operations
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Version with Markings to Show Changes Made

IN THE SPECIFICATION

Please amend the Specification as follows:

On page 1, after line 1 please insert the following heading:

--BACKGROUND OF THE INVENTION

Field of the Invention--;

On page 1, after line 5 please insert the following heading:

--Background of the Invention--;

On page 2, after line 12 please insert the following heading:

--Summary of the Present Invention--;

On page 3, after line 1 please insert the following heading:

--Brief Description of the Drawing Figures--;

On page 3, after line 7 please insert the following heading:

--Detailed Description of the Invention--.

Version with Markings to Show Changes Made

In the Claims

Please replace claims 1-5 and 7-9 with the following claims 1-5 and 7-9.

1. (Amended) An arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device, comprising:

a plurality of semiconductor switches, each having a first terminal, a second terminal and a third terminal;

a [first buss] control bus coupled to [a] said first [plurality of terminals] terminal of each of said plurality of semiconductor switches for communicating corresponding signals; and

a plurality of local [busses] buses that are separated from one another for communicating corresponding signals, a given one of said plurality of local [buss] buses having a first [buss] bus section coupled to [a] said second [plurality of terminals] terminal of respective ones of said plurality of semiconductor switches, each said first bus section [associated with said given local buss and] extending in a manner to cross [over] said [first] control [buss] bus and a second [buss] bus section [extending from] connected to said first [buss] bus section and having conductors thereof coupled [in a local, clustering buss arrangement] to the second terminals of [switches associated with said given local buss] the respective ones of said plurality of switches, the associated switches having the third terminals thereof coupled to the consecutively disposed column conductors[, respectively,] of [said] the array of the display device.

2. (Amended) An arrangement according to Claim 1 wherein said first plurality of terminals[, develop] receive switch control signals and said second plurality of terminals [develop] receive picture information signals for said switches [to form a demultiplexer] for storing the picture information in said pixels of said array.

3. (Amended) An arrangement according to Claim 1 wherein said associated switches including a plurality of sub-groups of switches, the switches of a given sub-group having the first terminals thereof coupled in common to a corresponding conductor of said

first [buss] bus and the third terminals thereof being coupled to consecutively disposed column conductors, respectively, of said array.

4. (Amended) An arrangement according to Claim 1 wherein the conductors of said second [buss] bus section of said given local [buss] bus are disposed [in a vicinity of] proximate said switches associated with said given [buss] bus and [remotely] remote from switches associated with the other local [busses] buses of said plurality of local [busses] buses to provide [buss] bus separation [for obtaining the local clustering buss arrangement].

5. (Amended) An arrangement according to Claim 1 wherein the conductors of said first [buss] bus extend along each of said plurality of semiconductor switches to form a global [buss] bus arrangement.

7. (Amended) A signal demultiplexer for a display panel, comprising:

a plurality of [clusters of switches] switch groups, each [cluster] switch group having ordinally numbered switches 1 thru n arranged sequentially, and each switch having respective input, output and control terminals with the control terminals of all switches in each [cluster] group connected to a common control terminal, and having respective output terminals coupled to successive data lines on [said] the display panel;

a plurality of [clusters] groups of data [busses] buses, each [cluster] group of data [busses] buses having ordinally numbered conductors 1 thru n, the ordinally numbered conductors of respective [clusters] groups of data [busses] buses being coupled to input terminals of corresponding ordinally numbered switches of a plurality of said [clusters of switches] switch groups;

a control [buss] bus including a plurality of conductors, said control [buss] bus arranged to [crossover] cross said plurality of [clusters] groups of data [busses] buses; and

connections between ones of said plurality of conductors of said control [buss] bus and respective common control terminals of said clusters of switches.

8. (Amended) A signal demultiplexer for a display panel, comprising:

a plurality of [clusters of switches] switch groups, a given [cluster] switch group having ordinally numbered switches arranged sequentially, and each switch having respective input, output and control terminals, the output terminals coupled to successive data lines on [said] the display panel;

a [cluster] group of data [busses] buses, a given data bus thereof having ordinally numbered conductors arranged sequentially, a given conductor of said given data [buss] bus being coupled in common to the input terminal of each switch having the same ordinal number that corresponds to the ordinal number of said given conductor and being included in each [cluster of said switches that is] switch group associated with said given data bus;

a control [buss] bus including a plurality of conductors, said control [buss] bus arranged to [crossover] cross said [clusters] group of data [busses] buses; and

connections between ones of said plurality of conductors of said control [buss] bus and respective control terminals of said [clusters of switches] switch groups.

9. (Amended) A signal demultiplexer according to Claim 8 wherein the control terminals of all the switches in each cluster of switches are connected in common to a corresponding conductor of said control [buss] bus.